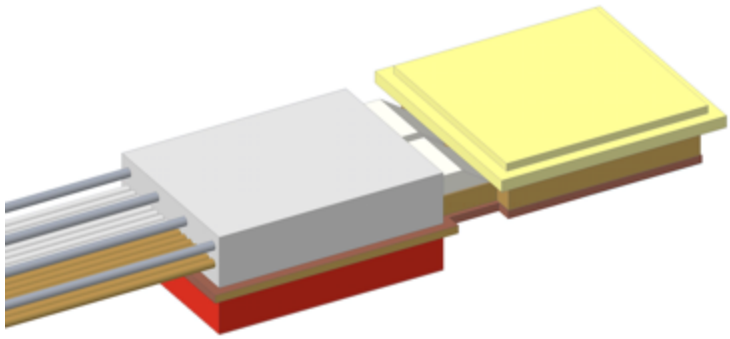
3.2 Tb/s Copackaged Optics
Optical Module
Product Requirements Document

Version 1.0
February 5, 2021



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CPO JDF

Revision	Date	Author	Notes
1.0	2/5/2021	J. Rahn	First draft for publication to JDF

1. Introduction

1.1. Scope

This document defines the technical specifications for a 3.2 Tb/s Copackaged Optic (CPO) transceiver module. This device will serve as a building block to enable a lower power solution for a 51.2Tb/s switch, with 16 modules arranged in close proximity to the switch ASIC. Two variants of the CPO module are defined in this document, one supporting 400GBASE-DR4 (with a total of 32 Tx/Rx fiber pairs), and one supporting 400GBASE-FR4 (8 Tx/Rx fiber pairs).

The document outlines our proposed architectural approach for a 51.2Tb/s switch. We anticipate having discussions with vendors to align with their technology platform capability. As such, significant changes could occur in the high-level requirements during that process. While specification tables, mechanical details and electrical pinouts are included for completeness, for this release, these tables should be regarded as placeholders as the system requirements are reconciled with hardware capability.

1.2. Introduction

The 3.2 Tb/s transceiver is a building block for a 51.2 Tb/s switch assembly. The block diagram for the overall system is shown in Figure 1. The transceiver module provides optical I/O to the switch ASIC via optical connections, and does conversion to short-reach electrical interfaces.

Details for the transceiver module are shown in Figure 2. The module includes digital signal processor (DSP), modulator driver and TIA chips, Silicon Photonics (SiPho) based optical transmitter and receiver. For the 400GBASE-FR4 variant, the module includes optical multiplexer (MUX) and de-multiplexer (DEMUX), and supports up to 3 km of duplex, single mode fiber. This module will be supported with two variants: one uses an external laser source (ELS) to provide the unmodulated light; the second relies on laser diodes built into the transceiver. For the latter configuration, the lasers need to have a backup laser in order to ensure adequate reliability of the full assembly.

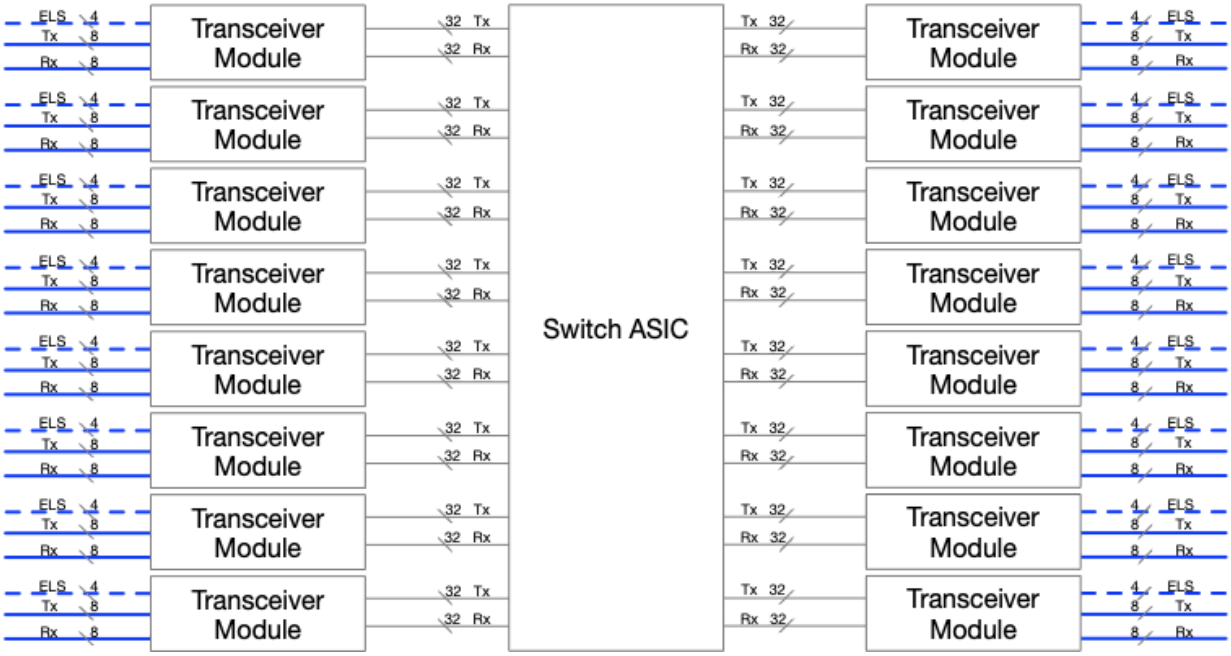

Figure 1. High-level system block diagram. Fiber counts shown are for 400GBASE-FR4; 400GBASE-DR4 has 32 fiber pairs per module.

The configuration shown in Figure 2 is logical; the vendor may arrange the DSP and transmit/receive lanes as appropriate, provided they support the inputs and outputs for the module, including optical, high-speed, DC, control, clock, etc. Given the high-density, integration of multiple functions and multiple 400G domains will likely be required.

The CPO transceiver subassembly will be mounted on a CPO substrate, which provides high-speed data path via XSR interfaces, and provides a limited set of power and control signals. A cross-section of the CPO assembly and transceiver is shown in figure 3. Transceiver cross-section is for illustrative purposes and vendor designs may vary.

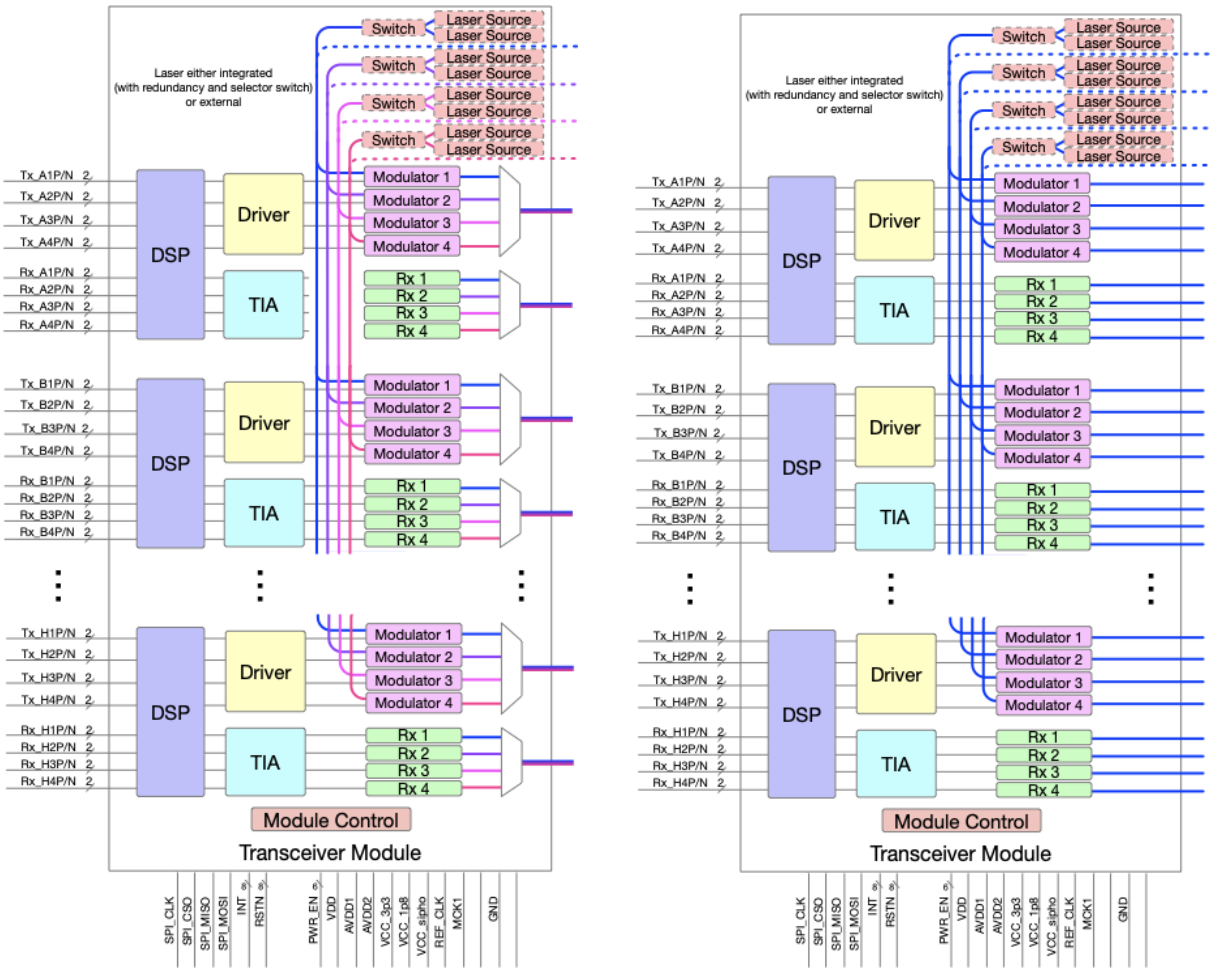

Figure 2. Functional block diagrams for transceiver module variants, with the left diagram showing 8×400GBASE-FR4, and right is 8×400GBASE-DR4. There are two options for the laser source: either integrated with redundant backup, or provided by an external laser source. Physical implementation of the ASICs likely will require more integration than shown in this functional diagram.

In 400G mode, the line side of the transceiver transmits and receives 8×400GBASE-FR4 or 8×400GBASE-DR4. The transceiver electrical interface facing the switch IC transmits and receives 32×106G electrical signals compliant to CEI-112G-XSR.

The 400GBASE-FR4 variant must support 200G operation. When configured for 200G, the line side of the transceiver transmits and receives 8×200GBASE-FR4. The transceiver electrical interface facing the switch IC transmits and receives 32×53G PAM4 electrical signals. In this case, the CEI-112-XSR interface should operate in a 53G/PAM4 mode.

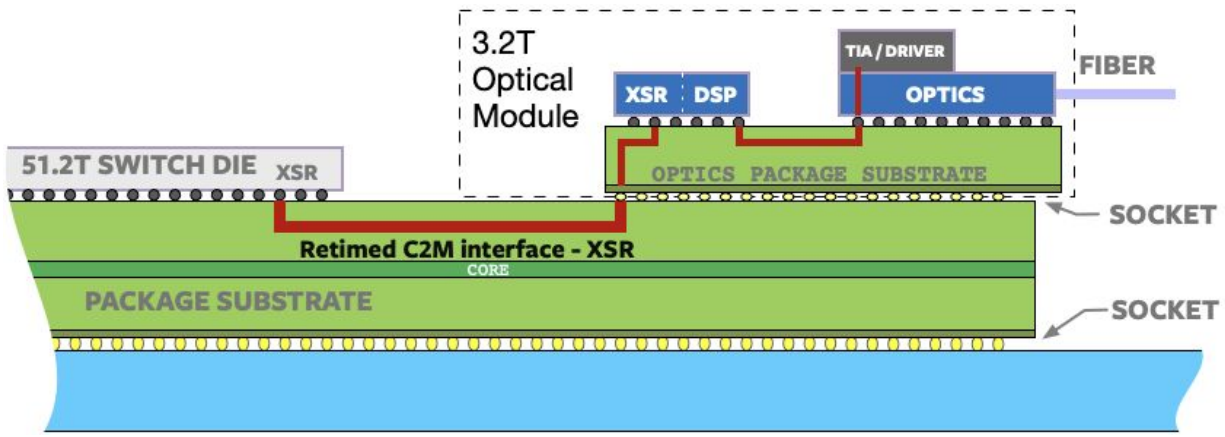

Figure 3. Cross-section of PCBA, CPO substrate, switch IC, and optical transceiver.

The transceiver shall have adequate margin to operate under the switch ASIC FEC BER threshold under specified conditions and over life. The architecture anticipates that the electrical signal gets retimed on both sides of the link, but FEC is only applied at the host (switch IC), as shown in Figure 4, following the IEEE 802.3 AUI definition.

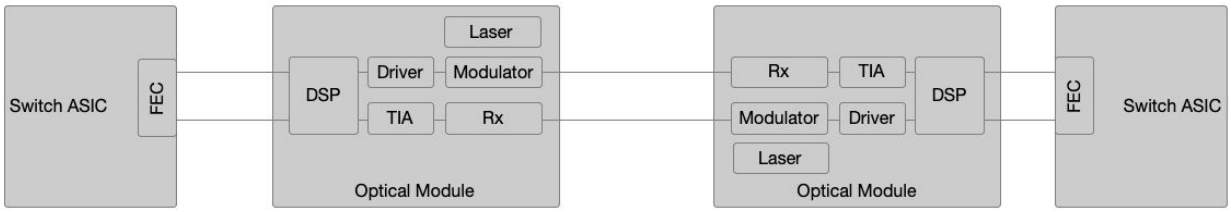

Figure 4. Arrangement of FEC correction.

1.3. Common Terms

The following terms are used in this document

- CPO – Co-Packaged Optics
- 200GE – 200 Gigabit Ethernet
- 400GE – 400 Gigabit Ethernet
- 400GBASE-FR4 – 400GE optical standard utilizing 4 wavelengths on a 1310nm CWDM grid with each wavelength transmitting 106.25Gb/s using 53.13Gbaud PAM4 modulation
- 200GBASE-FR4 - 200GE optical standard utilizing 4 wavelengths on a 1310nm CWDM grid with each wavelength transmitting 53.13Gb/s using 26.56GBaud PAM4 modulation
- 400GBASE-DR4 - 200GE optical standard utilizing 4 optical lanes operating at 1310nm, with each lane transmitting 106.25Gb/s using 53.13Gbaud PAM4 modulation
- QSFP56 – Quad Small Form-factor Pluggable (QSFP) operating at 4×56Gbps, used for 200GE
- QSFP-DD – Quad Small Form-factor Pluggable Double Density operating at

8×56Gbps, used for 400GE

- BER – Bit Error Rate
- ER – Extinction Ratio
- SMSR – Side Mode Suppression Ratio
- OMA – Optical Modulation Amplitude
- TDECQ – Transmitter and Dispersion Eye Closure Quaternary
- SECQ – Stressed Eye Closure Quaternary
- ESD – Electro-Static Discharge
- SiPho – Silicon Photonics
- TIA – Trans-impedance Amplifier
- MUX – Multiplexer
- DEMUX – De-multiplexer
- NRZ – Non-Return-to-Zero
- PAM – Pulse Amplitude Modulation
- DSP – Digital Signal Processor
- EBO – Extended Beam Optical Connector
- CEI-112G-XSR – Common Electrical Interface specification operating at a serial data rate of 112Gb/s over short reaches common in multi-chip modules
- CMIS – Common Management Interface Specification
- ESD – Electro-Static Discharge
- SPI – Serial Peripheral Interface
- LD – Laser Diode used as a CW source for the co-packaged optical module
- ELS – External Laser Source
- PMF – Polarization Maintaining Fiber

1.4. References

The following documents are referenced in generating this specification:

- IEEE 802.3bs – Media Access Control Parameters, Physical Layers and Management Parameters for 200 Gb/s and 400 Gb/s Operation; this amendment to 802.3 was adopted December 2017
- IEEE 802.3cu D2.2– Media Access Control Parameters, Physical Layers and Management Parameters for 100 Gb/s and 400 Gb/s over SMF at 100 Gb/s per Wavelength.
- OIF-CEI-x.x (CEI-112G-XSR currently in draft)
- CMIS revision 4.0 – Common Management Interface Specification

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Unit	Note
Storage temperature	T_st	-40		85	℃	
Relative humidity, storage and transportation	RH	5		85	%	Note1
ESD, low speed pins (<5Gbps)	ESD_HBM_low_speed			1000	V	Human body model
ESD, high speed pins (>5Gbps)	ESD__HBM_high_speed			500	V	Human body model
ESD, low speed pins (<5Gbps)	ESD_CDM_low_speed			250	V	Charged device model
ESD, low speed pins (>5Gbps)	ESD__CDM_high_speed			125	V	Charged device model
Power supply voltage	VDD	TBD		TBD	V	
	AVDD1	TBD		TBD	V	
	AVDD2	TBD		TBD	V	
	VCC_3p3	TBD		TBD	V	
	VCC_1p8	TBD		TBD	V	
	VCC_sipho	TBD		TBD	V	
SPI pins	V_SPI	-0.3		4	V	
Low speed control	RSTN, TXDIS, LoPWR	TBD		TBD	V	
Power supply control	VDD_EN, AVDDR_EN, V1P2_EN, V2P0_EN	TBD		TBD	V	
ELS port damage threshold				TBD	dBm	
Receive damage threshold	Pmax_rx			5.7	dBm	

Note:

1. The environment in which the module is operated must be controlled to prevent condensation. Compliance with ambient temperature and humidity limits defined in GR-63 is required.

Table 1. Absolute Maximum Ratings

3. Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Note
Signaling rate, each lane, 200GBASE-FR4 mode			26.5625		GBaud	+/-100ppm
Signaling rate, each lane, 400G mode			53.125		GBaud	+/-100ppm
Modulation format			PAM4			
Power supply range		-5%		5%	V	Supply Voltage > 3V
		-2.5%		2.5%	V	Supply Voltage≤ 3V
Module power supply noise tolerance, peak to peak	PSNR			2	%	Between 10Hz-10MHz
Operating case temperature, integrated laser	Tcase_int	15		70	°C	Note 1
Operating case temperature, external laser	Tcase_ext	15		85	°C	Note 1
Power consumption, integrated LDs	P			56	W	Tc = Max, End of Life
Power consumption, ELS	P			48	W	Tc = Max, End of Life
Relative humidity	RH	5		90	%	Note 2
Expected component lifetime	T_{OP}	TBD			Years	

Note:

1. Tcase to be measured in the middle of the top surface of the heat spreader. Module shall support loopback operation at TBD case temp for 12 hours. System integrator responsible for system level thermal solution.
2. Non-condensing. Transceiver shall also support up to 95% RH for up to 500hrs over life of component.

Table 2. Module Operating Condition

Supply Rail	Nominal	0.1 – 10 MHz	>10 MHz	<100 MHz	>100 MHz	AC	DC Level
VDD	TBD						±5%
AVDD1	TBD						±5%
AVDD2	TBD						±5%
VCC_3p3	TBD						±5%
VCC_1p8	TBD						±5%
VCC_sipho	TBD						±5%

Table 3. Power Supply Specification

Supply Rail	Nominal Voltage (V)	Current (A)		
		Min	Typical	Max (A)
VDD	TBD	---	---	TBD
AVDD1	TBD	---	---	TBD
AVDD2	TBD	---	---	TBD
VCC_3p3	TBD	---	---	TBD
VCC_1p8	TBD	---	---	TBD
VCC_sipho	TBD	---	---	TBD

Table 4 Supply Current Specification

4. Optical Characteristics

The optical specifications in general follow IEEE 802.3 as detailed below, unless this document specifies otherwise.

4.1. Optical Transmitter Characteristics for 200GBASE-FR4 Mode

Optical module shall comply with requirements defined in IEEE 802.3 specification, section 122.7.1.

4.2. Optical Transmitter Characteristics for 400GBASE-DR4 Mode

Optical module shall comply with requirements defined in IEEE 802.3 specification, section 124.7.1.

4.3. Optical Transmitter Characteristics for 400GBASE-FR4 Mode

Optical module shall comply with requirements defined in IEEE 802.3cu specification, section 151.7.1.

4.4. Optical Receiver Characteristics for 200GBASE-FR4 Mode

Optical module shall comply with requirements defined in IEEE 802.3 specification, section 122.7.1.

4.5. Optical Receiver Characteristics for 400GBASE-DR4 Mode

Optical module shall comply with requirements defined in IEEE 802.3 specification, section 124.7.2.

4.6. Optical Receiver Characteristics for 400GBASE-FR4 Mode

Optical module shall comply with requirements defined in IEEE 802.3cu specification, section 151.7.2.

4.7. External Light Source

For CPO designs which use an external light source, the following specifications apply. The light needs to be coupled into a PM fiber, which in turn is coupled to the CPO. Loss budget and tolerance likely need careful attention to enable appropriate output power. The light source will provide a small control range as a means to tune the modulated output power, which allows attenuation from the maximum power level.

The optical module indicates the presence of external light received via a digital signal, to enable eye safety interlock. Eye safety interlock control is pulled low when the optical module detects light on all four lanes, and ELS has pullup which disables light when the optical module is disconnected. ELS is responsible for powerup sequencing.

Parameter	Symbol	Min	Typical	Max	Unit	Note
FR4 Center Wavelength 1	FR-WL1	1265.25	1271	1276.75	nm	
FR4 Center Wavelength 2	FR-WL2	1285.25	1291	1296.75	nm	
FR4 Center Wavelength 3	FR-WL3	1305.25	1311	1316.75	nm	
FR4 Center Wavelength 4	FR-WL4	1325.25	1331	1336.75	nm	
DR4 Center Wavelength	DR-WL	1304.5	1311	1317.5	nm	
Optical power max per fiber	P_{ELS}	22		24	dBm	Note 1
Optical power control range	ΔP_{ELS}	6			dB	
Laser RIN	RINc	-141.5			dB/Hz	Note2
Laser SMSR	SMSR	30			dB	
Polarization Extinction Ratio	r_{ex}	16			dB	
Output reflectance	Rx_Ref			-26	dB	
Optical return loss tolerance				17.1	dB	

Notes:

1. With power control set for max power, the P_{ELS} can be any value between the min and max value
2. With -17.1dB reflection.

Table 6. External Light Source Specification

5. Electrical Specification

5.1. Electrical Connector

Electrical I/O connects from the assembly substrate into the photonic substrate via LGA pins on 0.6 mm pitch. Proposed electrical pinout is shown in figure 5 with pin assignments shown in figure 6. The pinout details are shown in Table 7-12. Pinout is preliminary and subject to change.

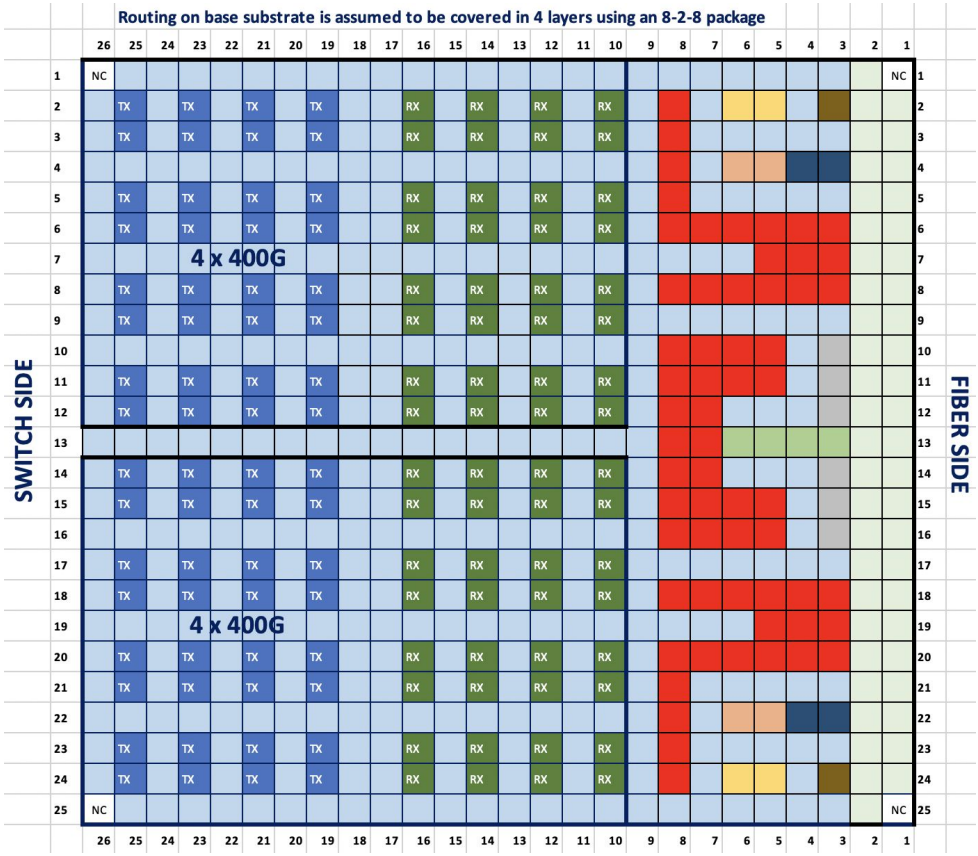

Figure 5. Electrical pins of 3.2 Tbs/s transceiver module

	# Pins		# Pins				# Pins
TX	64	VCC_3p3	2	VDD	60	SPI	4
RX	64	VCC_1p8	6	AVDD1	4	NC / No connect	4
Ground	386	VCC_sipho	4	AVDD2	4	TBD / TBD	48

Figure 6. Signals and power pin allocation for LGA pin-map.

Host Side Interface						
Signal Group	DS Net Name	LGA Net Name	Bump Net Name	Type	Count	Description
Electrical Data Input	RX_A[1:4][PN]	RX_A[1:4][PN]	RX_A[1:4][PN]	Input	8	Differential pair for RX data from HOST A – Lane 1 to 4
	RX_B[1:4][PN]	RX_B[1:4][PN]	RX_B[1:4][PN]	Input	8	Differential pair for RX data from HOST B – Lane 1 to 4
	RX_C[1:4][PN]	RX_C[1:4][PN]	RX_C[1:4][PN]	Input	8	Differential pair for RX data from HOST C – Lane 1 to 4
	RX_D[1:4][PN]	RX_D[1:4][PN]	RX_D[1:4][PN]	Input	8	Differential pair for RX data from HOST D – Lane 1 to 4
	RX_E[1:4][PN]	RX_E[1:4][PN]	RX_E[1:4][PN]	Input	8	Differential pair for RX data from HOST E – Lane 1 to 4
	RX_F[1:4][PN]	RX_F[1:4][PN]	RX_F[1:4][PN]	Input	8	Differential pair for RX data from HOST F – Lane 1 to 4
	RX_G[1:4][PN]	RX_G[1:4][PN]	RX_G[1:4][PN]	Input	8	Differential pair for RX data from HOST G – Lane 1 to 4
	RX_H[1:4][PN]	RX_H[1:4][PN]	RX_H[1:4][PN]	Input	8	Differential pair for RX data from HOST H – Lane 1 to 4
Electrical Data Outputs	TX_A[1:4][PN]	TX_A[1:4][PN]	TX_A[1:4][PN]	Output	8	Differential pair for TX data to HOST A – Lane 1 to 4
	TX_B[1:4][PN]	TX_B[1:4][PN]	TX_B[1:4][PN]	Output	8	Differential pair for TX data to HOST B – Lane 1 to 4
	TX_C[1:4][PN]	TX_C[1:4][PN]	TX_C[1:4][PN]	Output	8	Differential pair for TX data to HOST C – Lane 1 to 4
	TX_D[1:4][PN]	TX_D[1:4][PN]	TX_D[1:4][PN]	Output	8	Differential pair for TX data to HOST D – Lane 1 to 4
	TX_E[1:4][PN]	TX_E[1:4][PN]	TX_E[1:4][PN]	Output	8	Differential pair for TX data to HOST E – Lane 1 to 4
	TX_F[1:4][PN]	TX_F[1:4][PN]	TX_F[1:4][PN]	Output	8	Differential pair for TX data to HOST F – Lane 1 to 4
	TX_G[1:4][PN]	TX_G[1:4][PN]	TX_G[1:4][PN]	Output	8	Differential pair for TX data to HOST G – Lane 1 to 4
	TX_H[1:4][PN]	TX_H[1:4][PN]	TX_H[1:4][PN]	Output	8	Differential pair for TX data to HOST H – Lane 1 to 4

Table 7. High Speed Electrical Pins

Management Interface						
Signal Group	DS Net Name	LGA Net Name	Bump Net Name	Direction	Count	Description
SPI	SPI_CLK	SPI_CLK	SPI_CLK	Input	1	SPI Serial clock
	SPI_CSO	SPI_CSO	SPI_CSO	Input	1	SPI Chip Select. Additional chip select might be

						considered to support different implementations.
	SPI_MOSI	SPI_MOSI	SPI_MOSI	Input	1	SPI Master data output
	SPI_MISO	SPI_MISO	SPI_MISO	Output	1	SPI Master data input
Interrupt	INT[A:H]	INT[A:H]	INT[A:H]	Output	8	Interrupt output, Active low, for blocks A to H
Low Speed	RSTN[A:H]	RSTN[A:H]	RSTN[A:H]	Input	8	Master Reset, Active Low
	VDD_EN	VDD_EN	VDD_EN	Output	1	Host VDD supply control, Active high. Tie to GND if not used
	AVDDR_EN	AVDDR_EN	AVDDR_EN	Output	1	Host AVDDR supply control, Active high. Tie to GND if not used
	V1P2_EN	V1P2_EN	V1P2_EN	Output	1	Host 1.2V supply control, Active high. Tie to GND if not used
	V2P0_EN	V2P0_EN	V2P0_EN	Output	1	Host 2.0V supply control, Active high. Tie to GND if not used
	ELS1_EN	ELS1_EN	ELS1_EN	Output	1	External laser enable control for 1271 nm laser, low signal indicates presence of light
	ELS2_EN	ELS2_EN	ELS2_EN	Output	1	External laser enable control for 1291 nm laser, low signal indicates presence of light
	ELS3_EN	ELS3_EN	ELS3_EN	Output	1	External laser enable control for 1311 nm laser, low signal indicates presence of light
	ELS4_EN	ELS4_EN	ELS4_EN	Output	1	External laser enable control for 1331 nm laser, low signal indicates presence of light

Table 8. Low Speed Pins

Reference Clocks						
Signal Group	DS Net Name	LGA Net Name	Bump Net Name	Direction	Count	Description
	REF_CLK1_P	REF_CLK1_P	REF_CLK1_P	Input	1	Positive Terminal of Differential Reference Clock
	REF_CLK1_N	REF_CLK1_N	REF_CLK1_N	Input	1	Negative Terminal of Differential Reference Clock
	REF_CLK2_P	REF_CLK2_P	REF_CLK2_P	Input	1	Positive Terminal of

						Differential Reference Clock
	REF_CLK2_N	REF_CLK2_N	REF_CLK2_N	Input	1	Negative Terminal of Differential Reference Clock

Table 9. Reference Clock Pins

Lineside Monitor Clocks						
Signal Group	DS Net Name	LGA Net Name	Bump Net Name	Direction	Count	Description
	MCK1_P	MCK1_P	MCK1_P	Output	1	Positive Terminal of Monitoring Clock Output
	MCK1_N	MCK1_N	MCK1_N	Output	1	Negative Terminal of Monitoring Clock Output
	MCK2_P	MCK2_P	MCK2_P	Output	1	Positive Terminal of Monitoring Clock Output
	MCK2_N	MCK2_N	MCK2_N	Output	1	Negative Terminal of Monitoring Clock Output
Note: To reduce I/O count, DSP should have an internal mux such that any of the recovered clock signals can be monitored, with selection based on software control. One or both sets of monitor clock pins can be used as desired for the implementation.						

Table 10. Lineside Monitor Clock Pins

Miscellaneous						
Signal Group	DS Net Name	LGA Net Name	Bump Net Name	Direction	Count	Description
Vendor ID pins	VID_0	VID_0	VID_0	Output	4	Vendor ID PIN, GND or float per agreement
	VID_1	VID_1	VID_1	Output	4	Vendor ID PIN, GND or float per agreement

Table 11. Debug Pins

Power Supplies						
Signal Group	DS Net Name	LGA Net Name	Bump Net Name	Direction	Count	Description
Supplies	VDD	VDD	VDD	PWR	56	TBD
	AVDD1	AVDD1	AVDD1	PWR	4	TBD
	AVDD2	AVDD2	AVDD2	PWR	4	TBD
	VCC_3p3	VCC_3p3	VCC_3p3	PWR	2	TBD
	VCC_1p8	VCC_1p8	VCC_1p8	PWR	6	TBD
	VCC_sipho	VCC_sipho	VCC_sipho	PWR	4	Vendor defined supply
	GND	GND	VSS	GND	390	Ground

Table 12. Power Supply Pins

5.2. Low Speed PIN Electrical Specification

Low speed control and sense signal electrical specification is shown in Table 13. ModSelL pin will not be required as it will be included in the SPI bus (SPI chip select or SPI_CS). IntL and ResetL pins are required per 400G sub-module. Four power supplier control pins (VDD_EN, AVDDR_EN, V1P2_EN, V2P0_EN) are required for power sequencing control. 1.2V signals are used to optimize for high-speed CMOS.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
IO Supply Voltage	V_{cc}			1.2		V
Input/output capacitance	C_{IO}				6	pF
Input leakage current	I_{LI}				3.5	uA
Input Low Voltage	V_{IL}		-0.3		0.4	V
Input High Voltage	V_{IH}		0.7		1.5V	V
Output Low Voltage	V_{OL}		-0.2		0.3	V
Output High Voltage	V_{OH}		0.8		1.5V	V
Output High Current	I_{OH}		2			mA

Table 13. Low Speed Electrical Specification

5.3. High Speed PIN Electrical Specification

The ingress (Rx) high speed electrical interface from the switch ASIC shall be AC-coupled; the egress (Tx) will be AC coupled on the switch ASIC. The electrical specification shall be compliant to CEI-112G-XSR. Module vendors need to comply with the transmitter and receiver electrical compliance specification.

Output squelch upon receiver loss of signal (Rx LOS) or loss of lock (Rx LOL) is required. During normal operation, when Rx LOS or Rx LOL occurs on any optical channel, module firmware (FW) shall check the squelch setting of all Rx and squelch the lanes that have Rx

squelch enabled. Module FW shall do nothing for the lanes that have Rx squelch disabled. For any lane that is in the Rx squelch state, the output impedance levels are maintained while the differential voltage amplitude shall be less than the values defined in Table 14.

Tx squelch is also required. During normal operation, when the peak-to-peak electrical amplitude on any of the Tx input lanes from the switch ASIC is less than the input voltage level defined in Table 14, a Tx LOS will be triggered on that lane. Module FW shall check all the Tx and squelch the output of the channels that have Tx squelch enabled. Module FW shall do nothing for the channels that have Tx squelch disabled. For any channel in the Tx squelch state, the output optical power (AOP specifically) shall be turned off.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Differential peak-to-peak output voltage, at squelch				50	mV	
Differential peak-to-peak input voltage to trigger squelch				100	mV	

Table 14. Electrical Squelch Specification

5.4. Reference Clock Specification

Parameter	Conditions	Min	Typ	Max	Unit
Frequency[1]		---	156.25	---	MHz
Frequency Tolerance		---	---	100	ppm
Differential Swing	Peak-to-Peak	400	---	1600	mV
Single-ended Swing	Peak-to-Peak	200	---	800	mV
Duty Cycle		40	---	60	%
Rise Time	20% to 80%	---	---	400	ps
Fall Time	80% to 20%	---	---	400	ps
AC Coupling1		---	100	---	nF
RMS Jitter	12 kHz – 1 MHz			120	fs
	1 MHz – 20 MHz			150	fs
	12 kHz – 20 MHz			220	fs
Note: 1. The 156.25 MHz and 100 nF are the only values supported					

Table 15. Reference Clock Specification

5.5. Timing Requirements for Control and Status

Table 16 shows timing requirements for control and status information of CPO module. It matches QSFP-DD specification with addition of following:

1. Serial bus hardware ready time
2. Monitor data ready time

3. Reset assert time
4. LPMode assert time
5. LPMode de-assert time
6. Application or rate select change time

Parameter	Symbol	Min	Typ	Max	Unit	Note
MgmtInit duration	t_init			2000	ms	
Reset init assert time	t_reset_init	10			us	
Serial bus hardware ready time	t_serial			2000	ms	Note1
Monitor data ready time	t_data			2000	ms	Note2
Reset assert time	t_reset			3000	ms	Note3
LPMode assert time	toff_LPMode			100	us	Note4
LPMode de-assert time	ton_LPMode			3000	ms	Note5
IntL assert time	ton_IntL			200	ms	
IntL de-assert time	toff_IntL			500	us	
Rx LOS assert time	ton_LOS			100	ms	
Tx fault assert time	ton_flag			200	ms	
Flag assert time	ton_flag			200	ms	
Mask assert time	ton_mask			100	ms	
Mask de-assert time	toff_mask			100	ms	
Application or rate select change time	t_ratesel			100	ms	
Module select wait time	ModSelL_WaitTime		N/A			
DataPathDeinit max duration	DataPathDeinit_MaxDuration		TBD			
DataPathInit max duration	DataPathInit_MaxDuration		TBD			
ModulePwrDn max duaration	ModulePwrDn_MaxDuration		TBD			
Rx squelch assert time	ton_Rxsq			100	ms	
Rx squelch de-assert time	toff_Rxsq			2000	ms	
Tx squelch assert time	ton_Txsq			400	ms	
Tx squelch de-assert time	toff_Txsq			2000	ms	
Tx disable assert time	ton_txdis			100	ms	
Tx disable de-asssert time	toff_txdis			400	ms	
Rx output disable assert time	ton_rxdis			100	ms	
Rx output disable de-assert time	toff_rxdis			100	ms	
Squelch disable assert time	ton_sqdis			100	ms	
Squelch disable de-assert time	toff_sqdis			100	ms	

ELS interlock report	ilk_det			1	ms	Note 6

Note:

1. Time from power on until the module responds to data transmission over the SPI bus.
2. Time from power on until DDM updates start and reflect accurate values.
3. Time from ResetL rising edge to module operational.
4. Time from LPMode rising edge to module achieves ModuleLowPwr state.
5. Time from LPMode falling edge to module achieves ModuleReady state.
6. Time from optical loss of signal to pin deassert.

Table 16. Timing Requirements for Control and Status

6. Mechanical

The CPO assembly consists of a high-density organic substrate, switch IC and optical modules arrayed around the perimeter. The mechanical layout of the CPO assembly is shown in Figure 7.

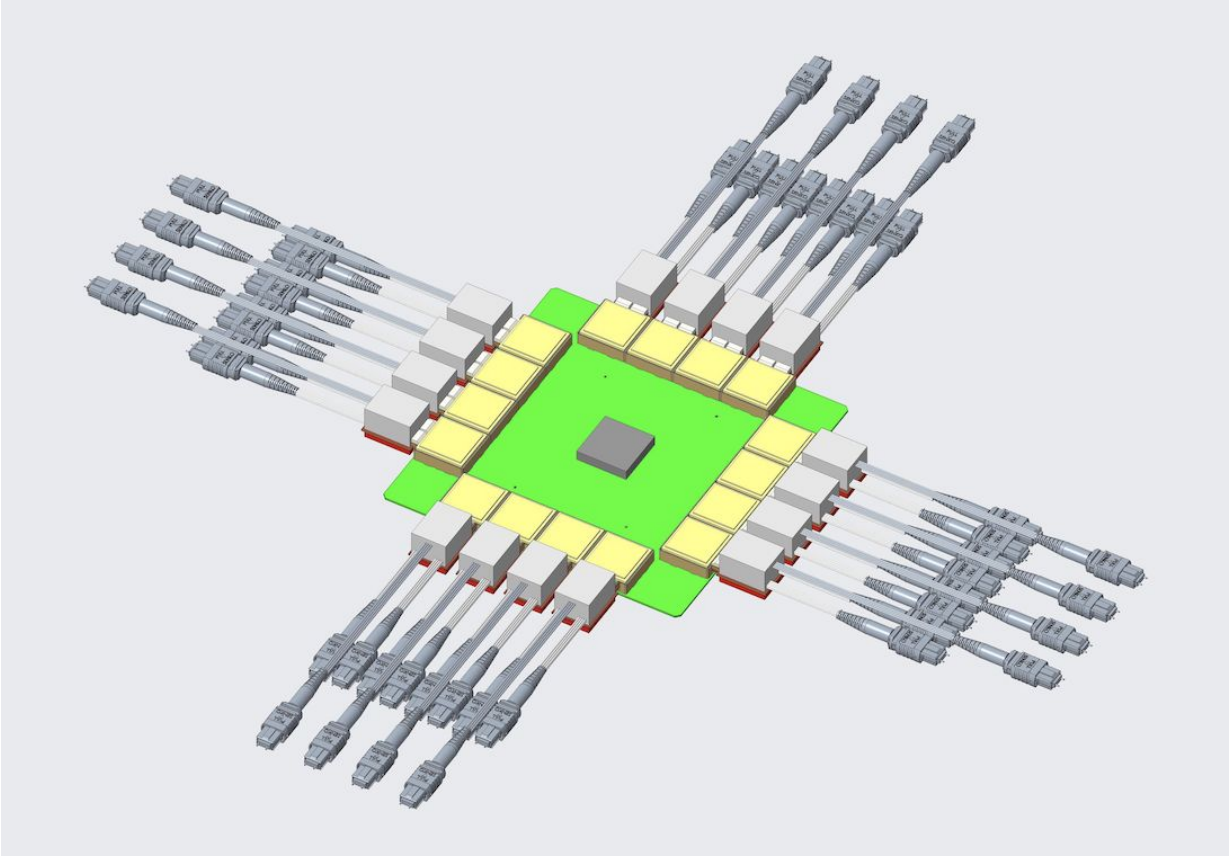

Figure 7. Full assembly of copackaged switch, showing sixteen transceiver modules.

Mechanical drawing of the transceiver module is shown in Figure 8. The goal is to meet the overall dimensions of the assembly, but note that there is some freedom to use additional space by extending the optical assembly beyond the edge of the CPO substrate.

The optical connectors provide a means to connect the optical module to the front plate of the line card or device. The optical module may be pigtailed or have an integrated optical connector. For a module with an integrated optical connector(s), an optical patch cord would be used to connect the optical module to the faceplate of the switch.

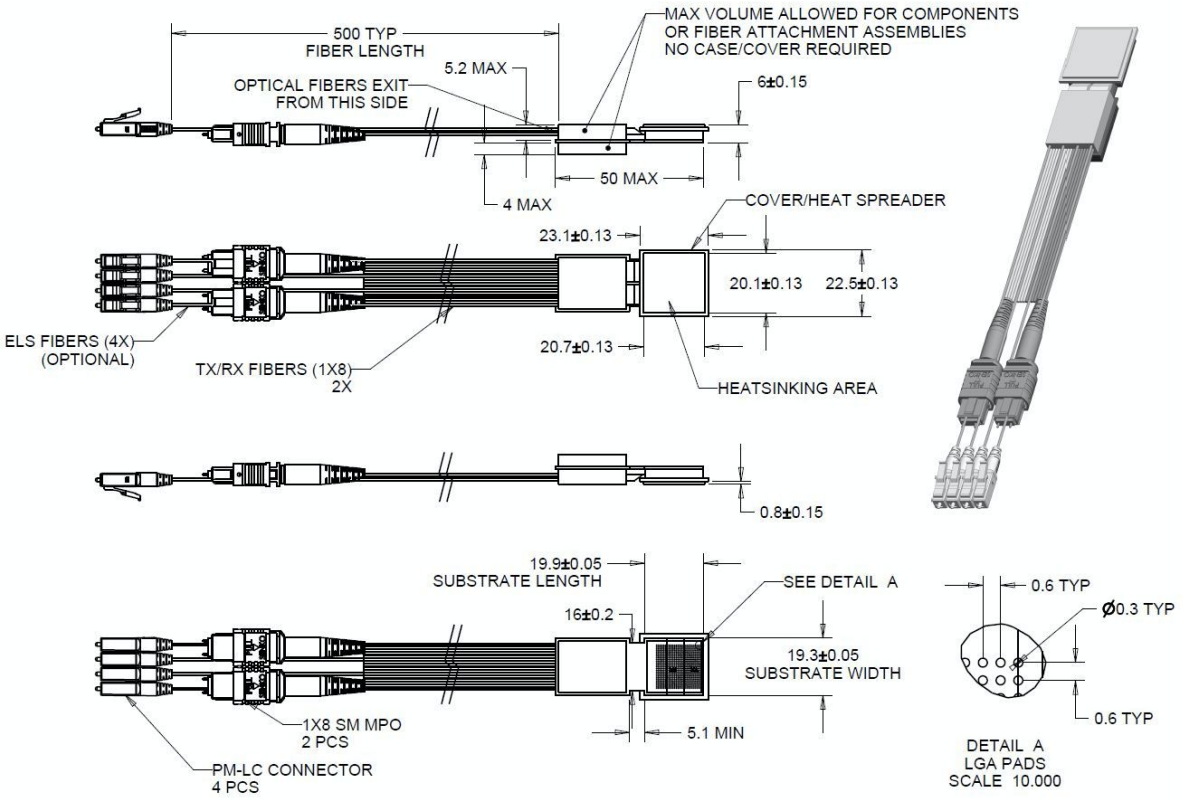

Figure 8. CPO transceiver module mechanical dimensions, for 400GBASE-FR4 variant of module with external lasers. For internal lasers, the PM-LC fibers will not be present. For 400GBASE-DR4, Tx/Rx fiber count will be 4x higher as detailed in section 6.2.

6.1. Optical Connectors: 400GBASE-FR4

The pig-tailed version would have SMF ribbons for the Tx and Rx terminated in a high-density optical connector. The 8×400GBASE-FR4 module has 8 fibers for the Tx and 8 fibers for the Rx functions. Here two 1×8 parallel fiber arrays exit the module and each is terminated in a 1×8 MPO connector. This arrangement could be replaced by a single 1x16 MPO connector if preferred. The MPO connector would be attached to a bulk-head adaptor inside the switch.

6.2. Optical Connectors: 400GBASE-DR4

The 8×400GBASE-DR4 module has 32 fibers for the Tx and 32 fibers for the Rx functions. Eight 1×8 parallel fiber arrays exit the module and each is terminated in a 1×8 MPO connector. This arrangement could be replaced by four 1x16 MPO connectors if preferred. Again, the MPO connector would be attached to a bulk-head adaptor inside the switch system.

6.3. Optical Connectors to External Laser Source

Some CPO designs will rely on an External Laser Source (ELS) to provide a CW light source to the optical modules. Light from the ELS assembly will be coupled via four polarization maintaining fibers assembled into a ribbon. On the transceiver module, each CW source will be split and distributed to eight transmitters. In this scenario, the laser source would have 9 dB of splitting loss and 3 dB of modulation loss, with the balance of the input power to output power allocated to excess loss due to coupling into and out of the transceiver module, and excess loss from splitters, waveguides, modulator, and mux.

Polarization Maintaining Fiber (PMF) is required for providing the external light source to the CPO assembly. The transceiver module will require 4 ELS fibers, terminated with a keyed LC connector to accommodate the PMF.

6.4. Thermal Considerations

To interface with the cooling element, the optical modules will incorporate a heat spreader on the top surface. A Thermal Interface Material (TIM) will be used between the cooling element and the module's heat spreader. To maximize cooling efficiency and minimize module case temperature, the optical module's heat spreader flatness should be as uniform as possible across the CPO assembly. As shown in Figures 7 & 8, a heat spreader of 20 mm on each side acts as the thermal interface.

For initial design guidance, the vendor should assume that all heat from the transceiver module will be removed through the heat spreader (all other surfaces, including the LGA pins, are adiabatic). The vendor can assume the switch heat sink will keep the heat spreader surface below the maximum specified case temperature shown in Table 2.

7. Environmental and Thermal

Parameter	Symbol	Min	Typical	Max	Unit	Note
Altitude, during operation, relative to sea level		-50		1800	m	
Acoustic, during operation		55			dBA	Note1
Altitude, storage, to sea level				5	km	
Altitude, transportation, to sea level				12	km	
Gaseous contamination						Note2

Assembly cycles		TBD				Note3
Optical assembly cycles		TBD				Note3

Note:

1. Refer to IEC 68-2-36, IEC 68-2-6
2. Conform to Severity Level G1 per ANSI/ISA 71.04-1985.
3. Number of cycles of mount/unmount from CPO substrate
4. Number of cycles of connect/disconnect of optical patch cables

Table 17. Environmental Regulation Requirement

8. Management Interface

8.1. Management Interface

The management interface proposed is the same specification used for 400G pluggable modules, QSFP-DD Common Management Interface Specification (CMIS). The current CMIS covers 16 lanes and there is a desire to extend this to 32 for applications like CPO. Optical modules with >32 lanes will require multiple instances of CMIS. One Serial Peripheral Interface (SPI) will be used for each CMIS instance. A preliminary SPI access protocol proposal is shown below Table 18. SPI interface should operate with a clock frequency ≥ 20MHz. SPI timing is detailed in Figure 8.

Byte#	Write value	Read value
0	Command [7]: Transfer direction 0 = Read 1 = Write [6:0]: # of bytes to transfer – 1 (0=1 byte, 0x7f = 128 bytes)	Reserved
1	[7:2] Reserved [1:0] Bank select	Reserved
2	Page number, ignored if register address number < 0x80	Reserved
3	Register address number	Reserved
4	0x00	Reserved
5	0x00	Write ready 0xFF: write busy 0x00: write ok
6	Write data byte1	Read data byte 1
7..133	Write Data byte 2… (up to 128)	Read data byte 2… (up to 128)

Table 18. SPI Access Protocol

8.2. SPI Interface Timing

The SPI interface timing is shown in Table 19.

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock Frequency	f_{SCK}		0.1	16	MHz
Data set-up time	t_{DS}		4		ns
Data hold time	t_{DH}		0		ns
Data output valid time	$t_{V(Q)}$		21	22	ns
Back to back timing1	t_{BB}		5		us
Slave select timing	t_{SS}		62.5		ns

Table 19. SPI Timing Specification

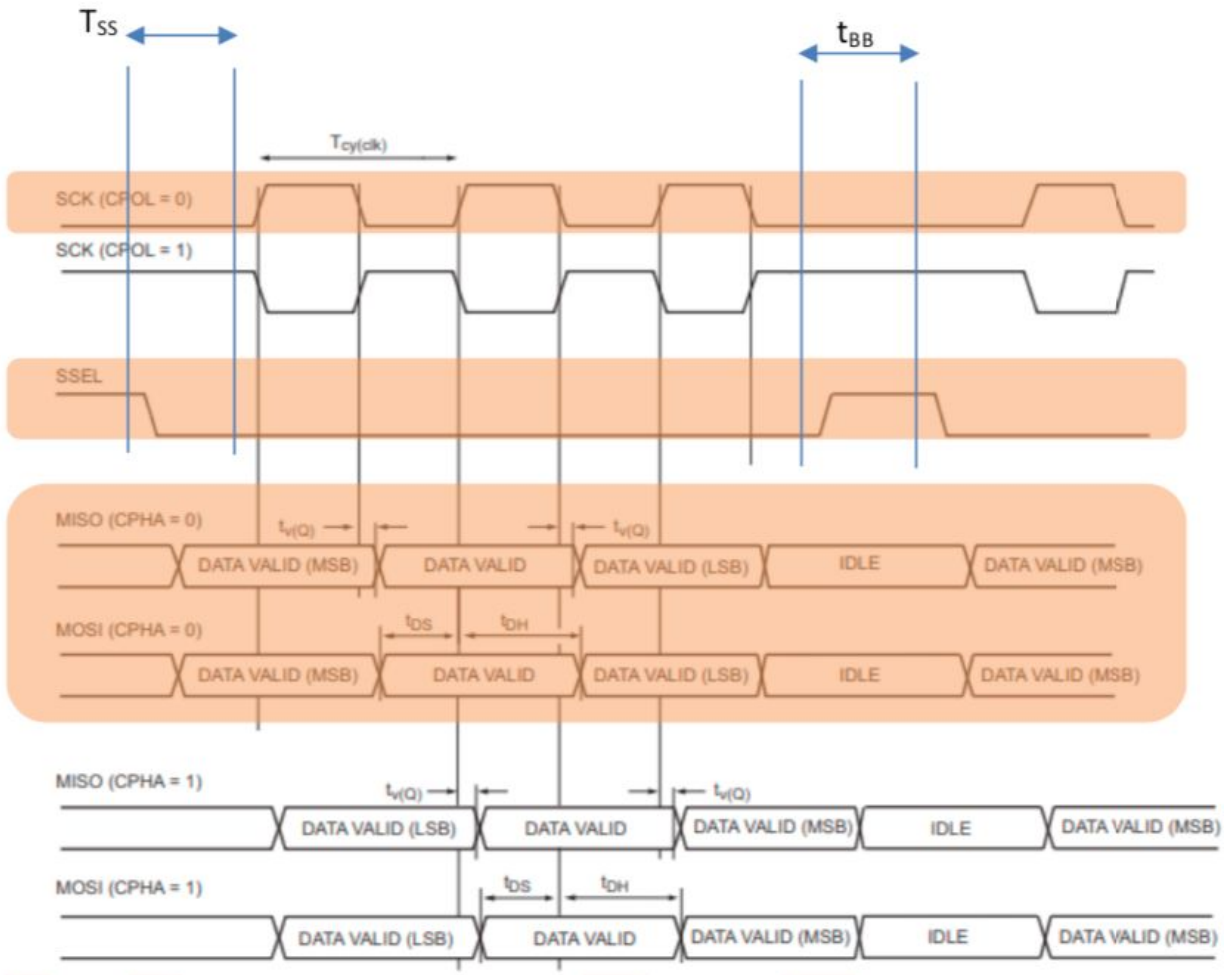

Figure 8. SPI timing diagram

8.3. Alarm and Warning Settings

Alarms and warnings are to be set to the same level. High/low levels are selected to be outside the specified operating range such that if triggered, action is required.

Parameter	High Alarm	Low Alarm	High Warning	Low Warning	Unit	Note
Case temperature	65	10	65	10	°C	
Voltage	Vmax+10%	Vmin-10%	Vmax+10%	Vmin-10%	V	
Tx output optical power, each lane	6.7	-7.2	6.7	-7.2	dBm	
Rx outer optical modulation amplitude, each lane	6.5	-40	6.5	-40	dBm	Note1
Tx laser current	Vendor specific	Vendor specific	Vendor specific	Vendor specific	mA	Note2

Note:

1. Rx LOS is used for low Rx signal strength indicator. The low alarm/warning should never be triggered
2. The alarms/warnings are to be defined by each vendor, but should follow the same principles shown above

Table 20. Alarm and Warning Settings

8.4. Equalizer Settings

CPO module shall use DSP to regenerate electrical signals on ingress from switch IC and egress to switch IC. The DSP equalization setting is shown in Table 21. DSP ingress (Rx) shall support adaptive equalization.

Transceiver DSP setting	Min	Typical	Max	
Switch IC ingress equalization	NA	NA	NA	Host ingress to use adaptive equalization
Switch IC egress de-emphasis	TBD	TBD	TBD	
Switch IC egress peak-to-peak amplitude	TBD	TBD	TBD	

Table 21. Transceiver Equalization Settings

9. Labels and Marking

TBD

10. EMC

Vendor will provide an EMC report from a certified test lab. Module EMC report will include the following tests.

1. Radiated emissions
2. Electrostatic discharge immunity
3. Radiated EM field immunity

Testing must be conducted on a minimum of two modules and may be tested in a vendor-designed, 1-up test fixture. For testing on an individual module, radiated emissions must comply with CISPR 22 (EN55022) for class B products. ESD and radiated immunity must comply with CISPR 24 (EN55024). For ESD immunity, test level 4 is to be used.

In addition to vendor EMC testing, customer will conduct radiated emission testing on fully loaded switches in an internal or external compliance lab to CISPR 22 (EN55022) class A limits. It is required that the vendor's modules are compliant in switch-level testing as well.

11. Quality and Reliability

The CPO FIT rates will be specified to guarantee an AFR of <1% for the 51T CPO-based switch. This will require some adjustment to the FIT levels at the 3.2T optical level.

12. Digital Diagnostic Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Reported case temperature accuracy	Tcase_Err	-3		3	°C
Reported voltage accuracy	Vcc_Err	Vtyp-2%		Vtyp+2%	mV
Reported Tx output power accuracy	Pout_Err	-2		2	dB
Reported Rx input power accuracy	Pin_Err	-2		2	dB
Reported Tx bias current accuracy	Ibias_Err	-10		10	%

Table 22. Digital Diagnostic Specification